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(54) ORGANIC LIGHT EMITTING DISPLAY DEVICE AND METHOD FOR MANUFACTURING THE SAME

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(57) **ABSTRACT**

Disclosed is an organic light emitting display device including a thin film transistor on a substrate, a planarization layer on the thin film transistor, a contact hole passing through the planarization layer to expose a source or drain electrode of the thin film transistor, a first electrode on the planarization layer, the first electrode being connected to the source or drain electrode of the thin film transistor through the contact hole, a hole between the first electrode and another first electrode adjacent thereto, the hole being a recessed portion of the planarization layer, a pixel defining layer covering the first electrode passing through the contact hole and the planarization layer disposed in the hole, a light emitting layer on the first electrode and the pixel defining layer, and a second electrode on the light emitting layer.

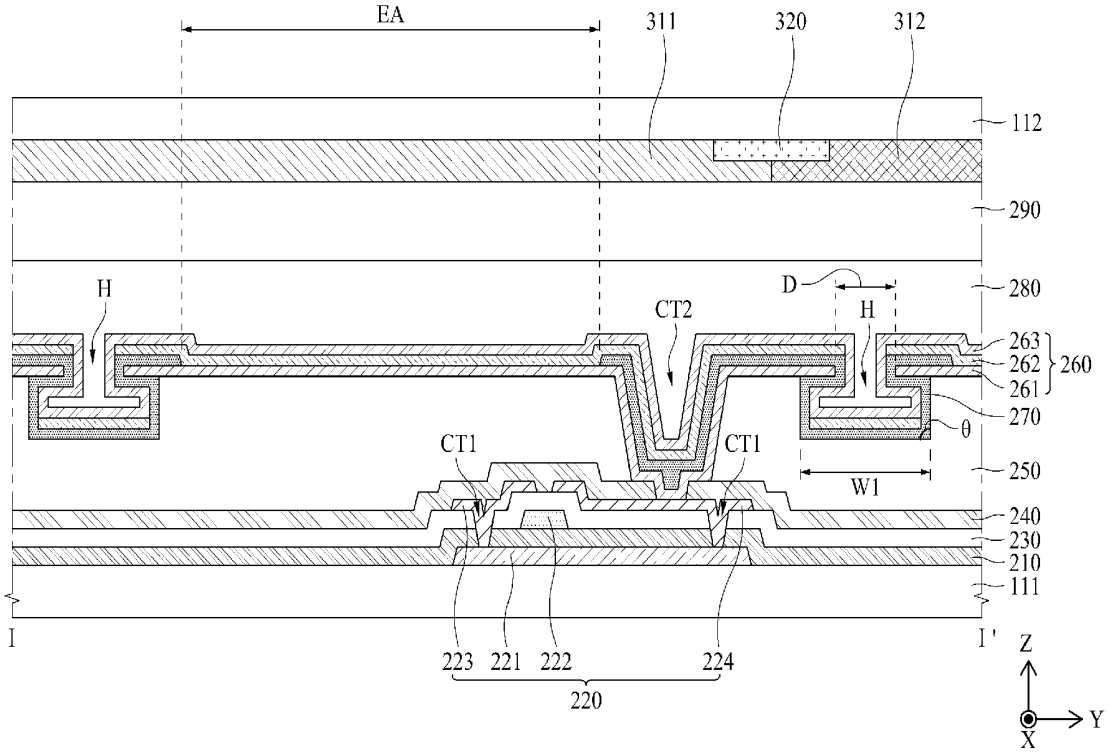

FIG. 1

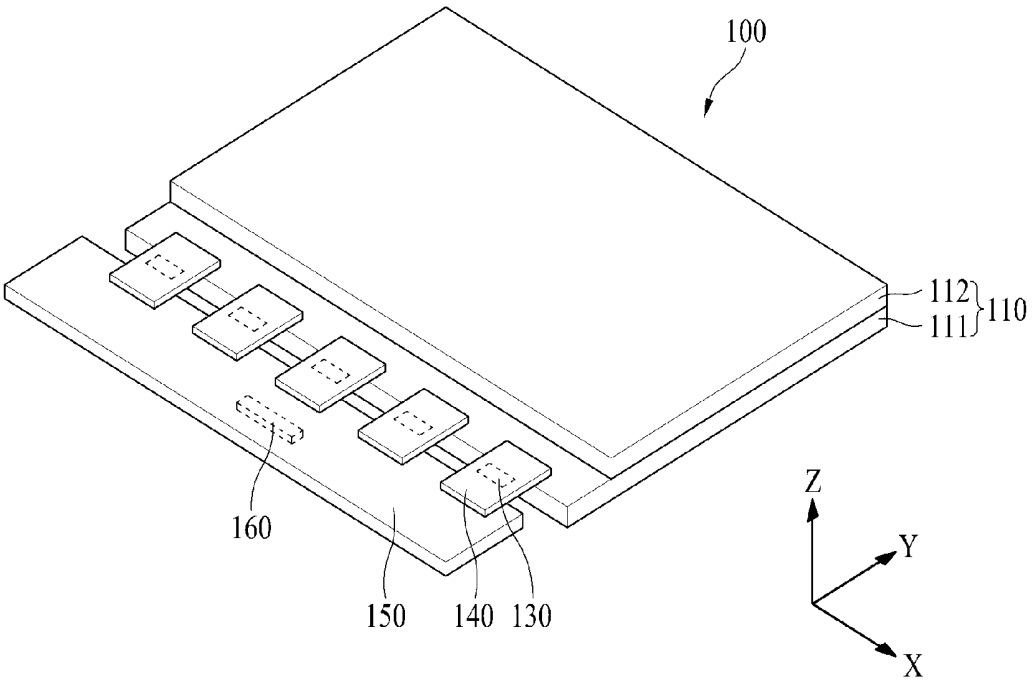
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FIG. 2

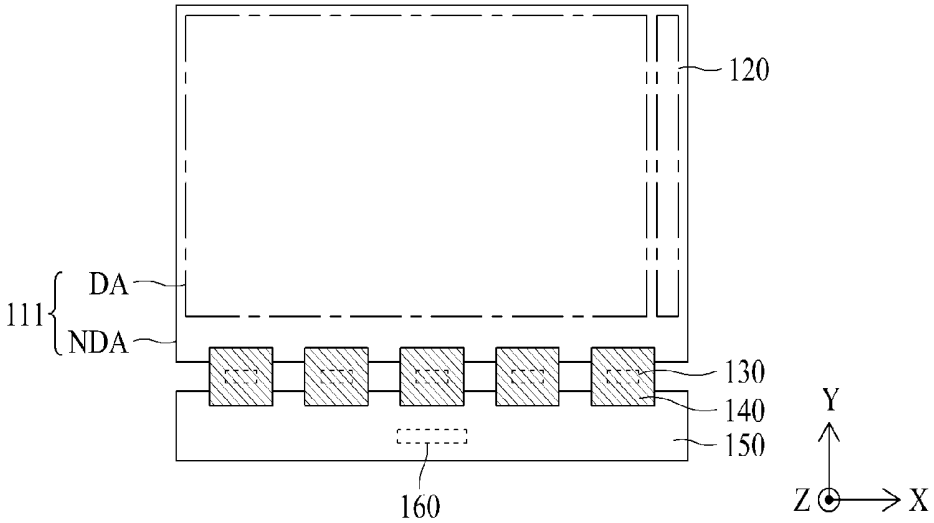
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FIG. 3

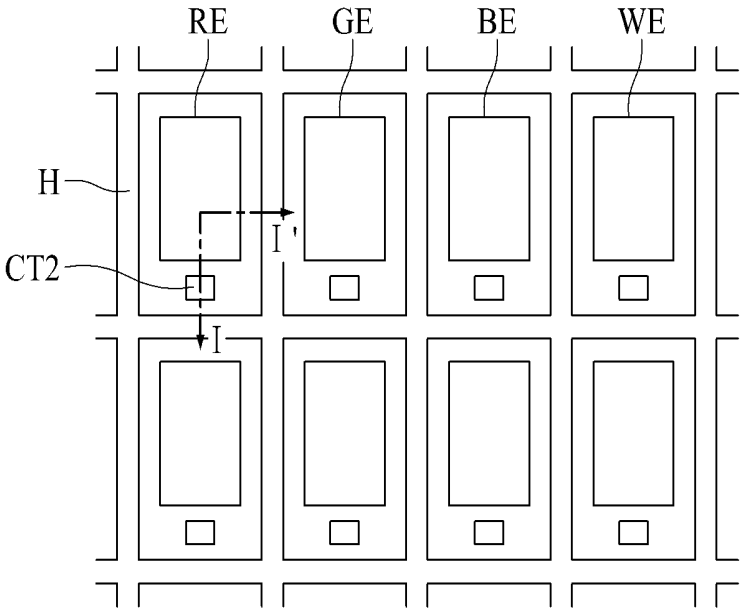

FIG. 4

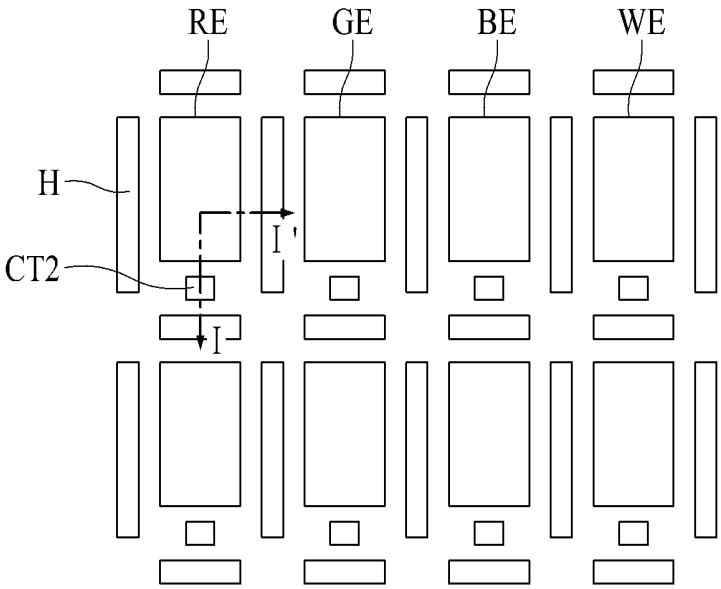

FIG. 5

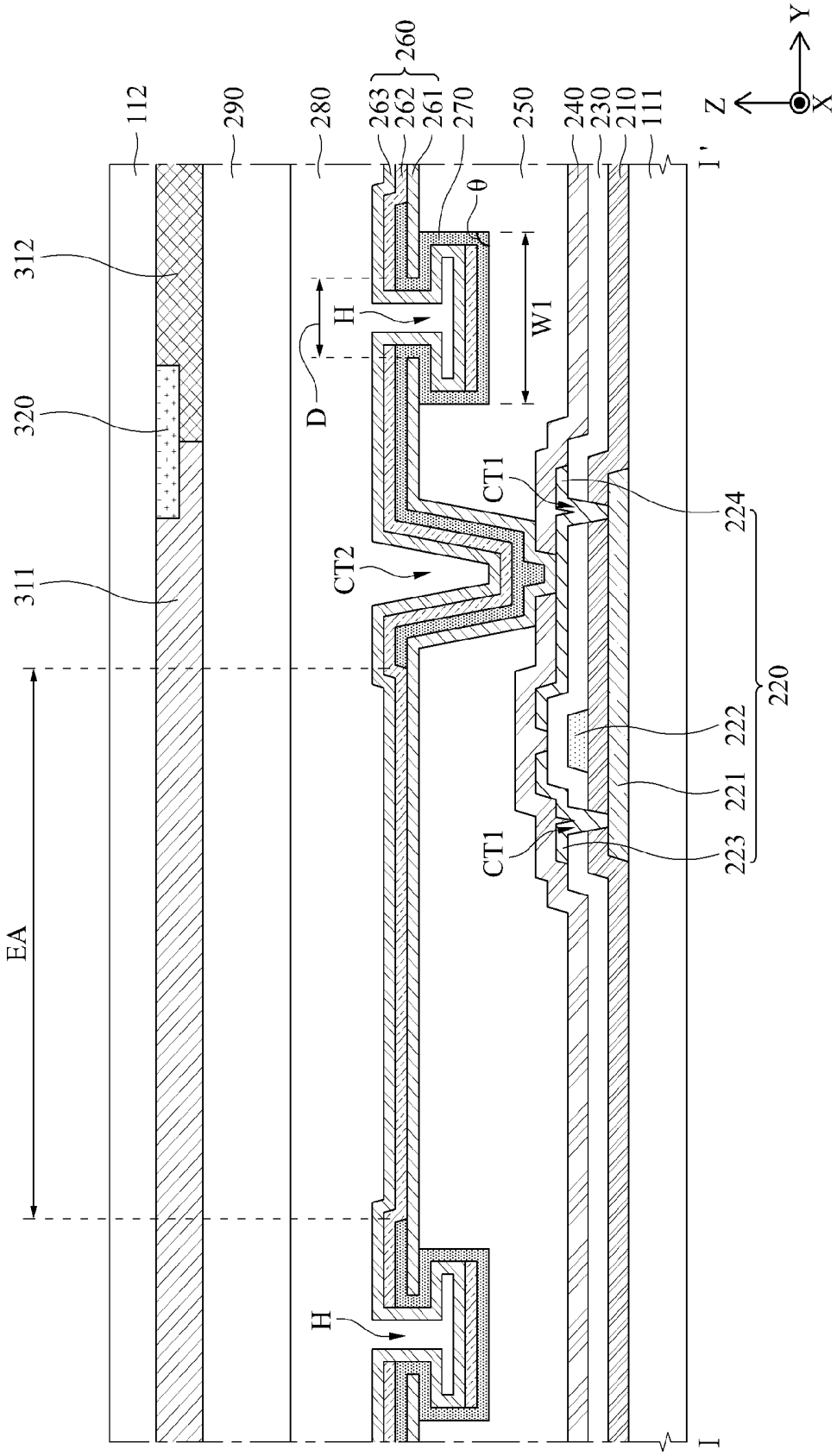
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FIG. 6

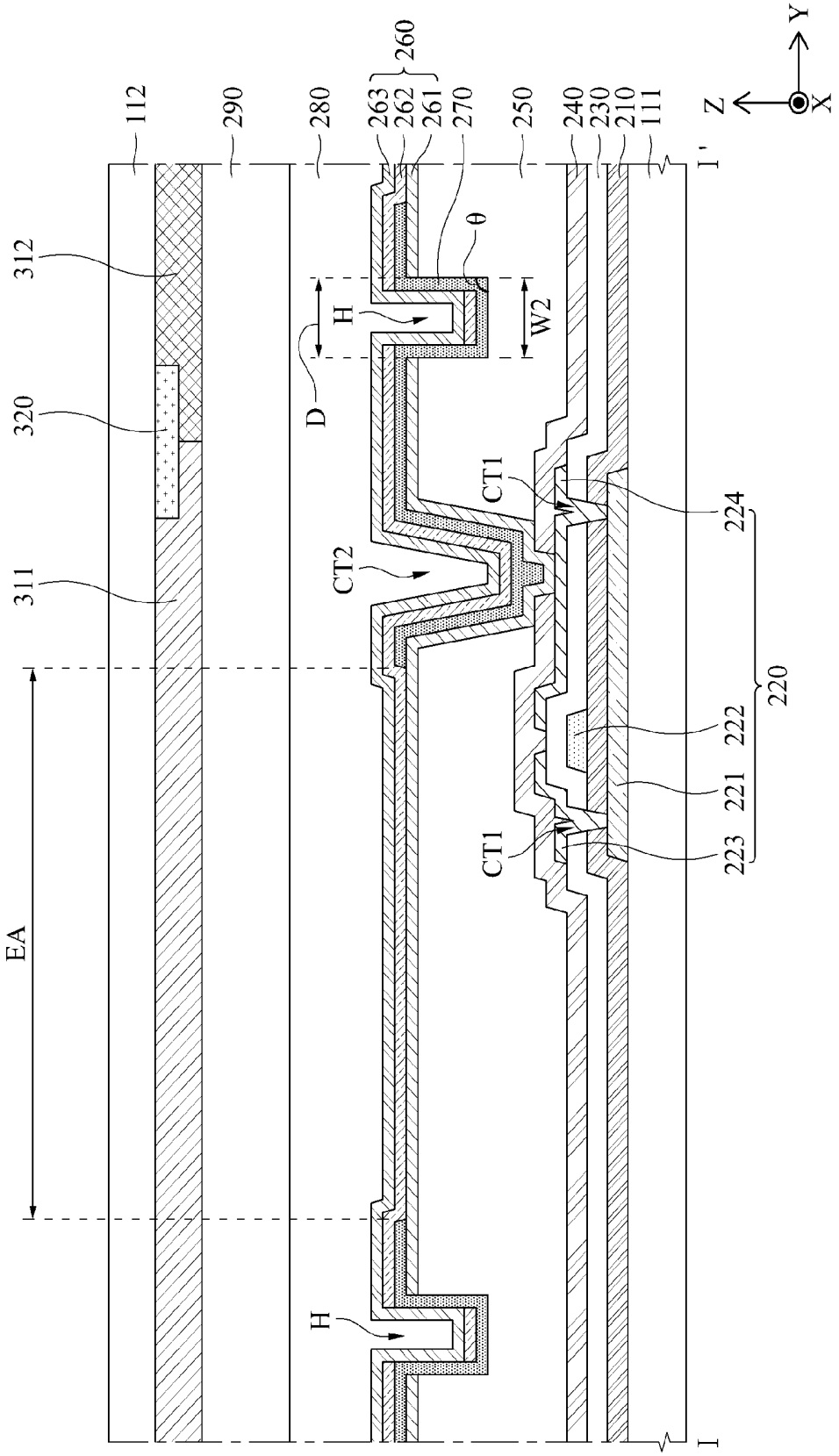
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FIG. 7

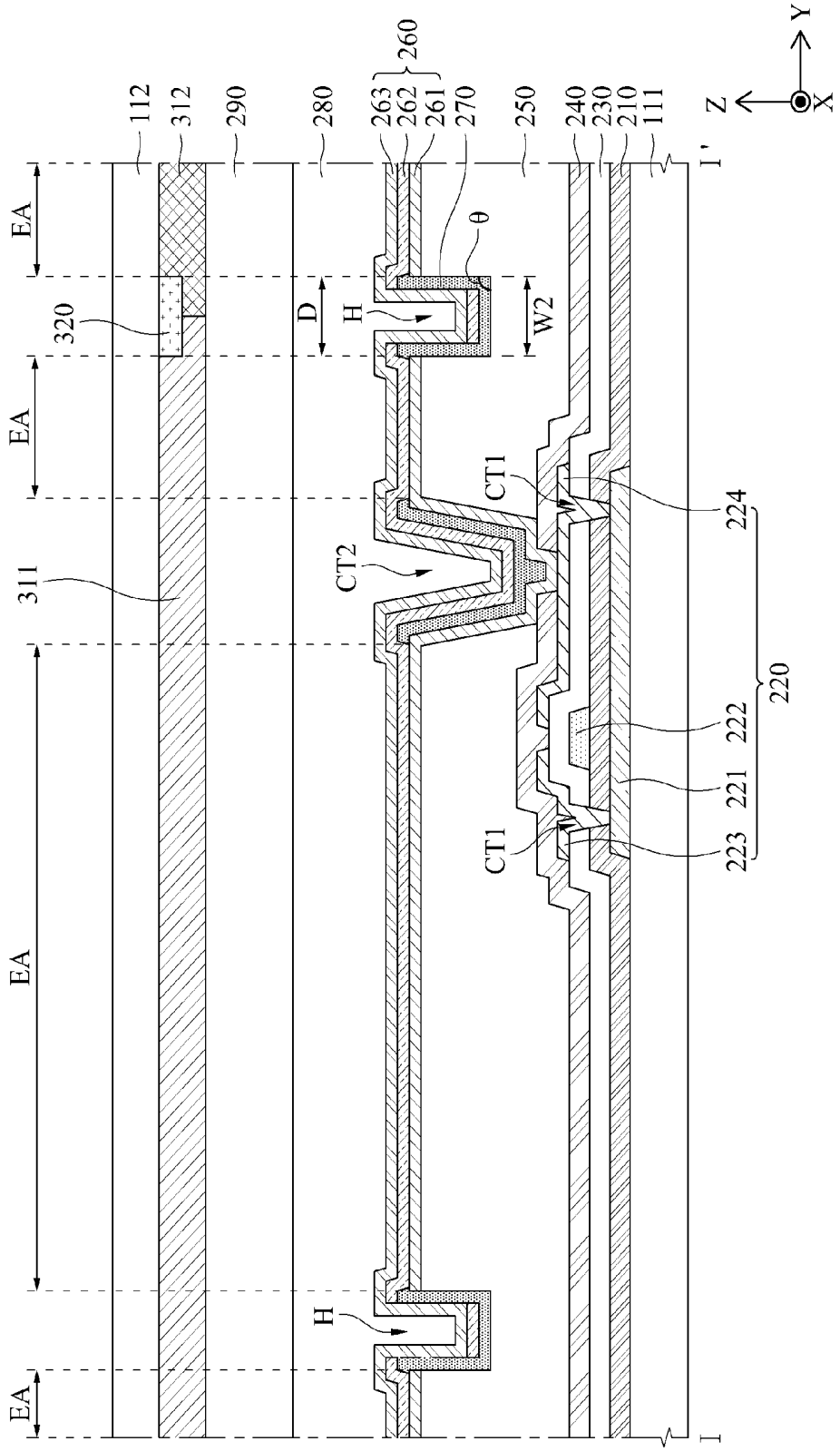
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FIG. 8

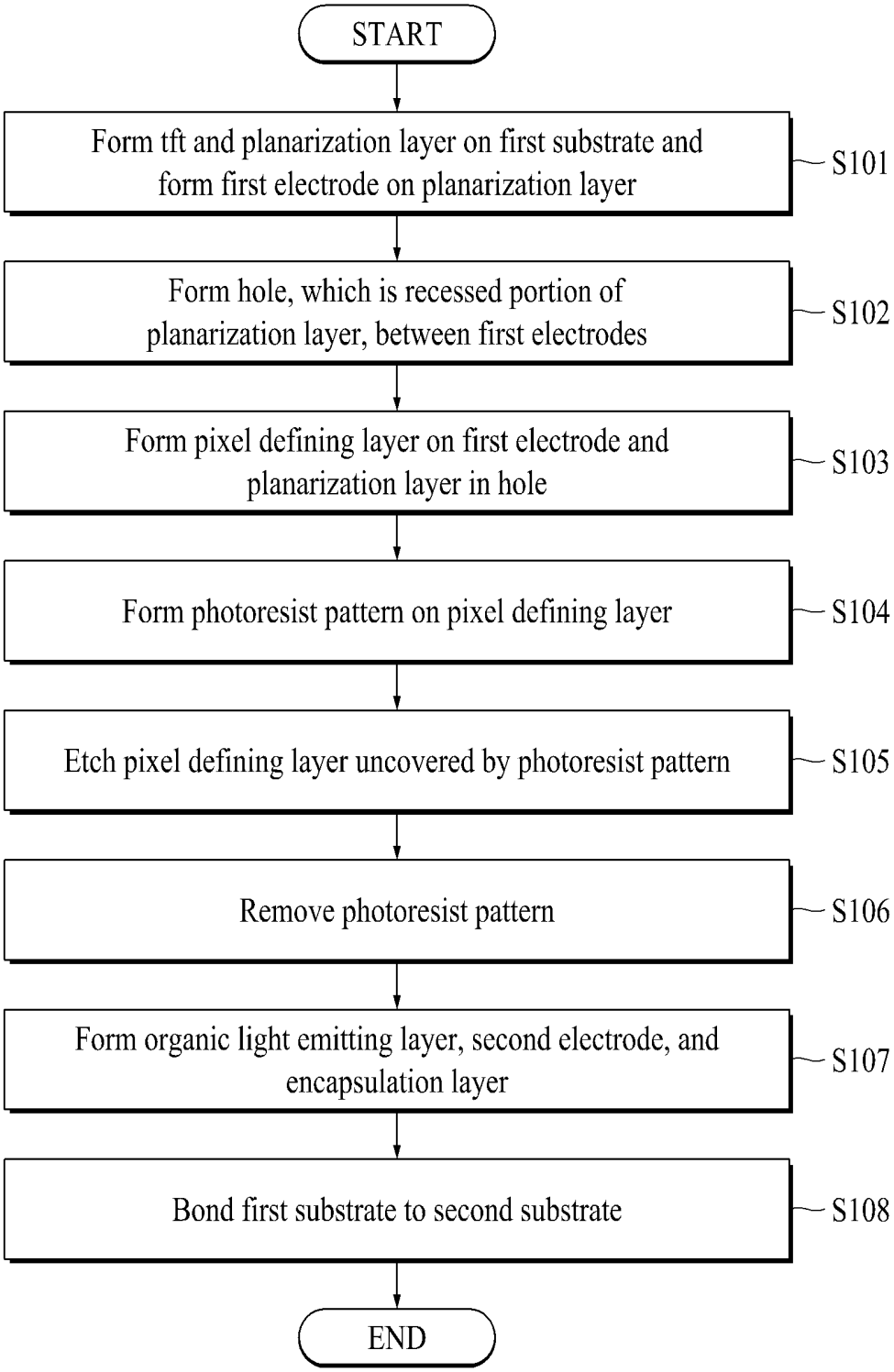
START
Form tft and planarization layer on first substrate and form first electrode on planarization layer
S101
Form hole, which is recessed portion of planarization layer, between first electrodes
S102
Form pixel defining layer on first electrode and planarization layer in hole
S103
Form photoresist pattern on pixel defining layer
S104
Etch pixel defining layer uncovered by photoresist pattern
S105
Remove photoresist pattern
S106
Form organic light emitting layer, second electrode, and encapsulation layer
S107
Bond first substrate to second substrate
S108
END

FIG. 9A

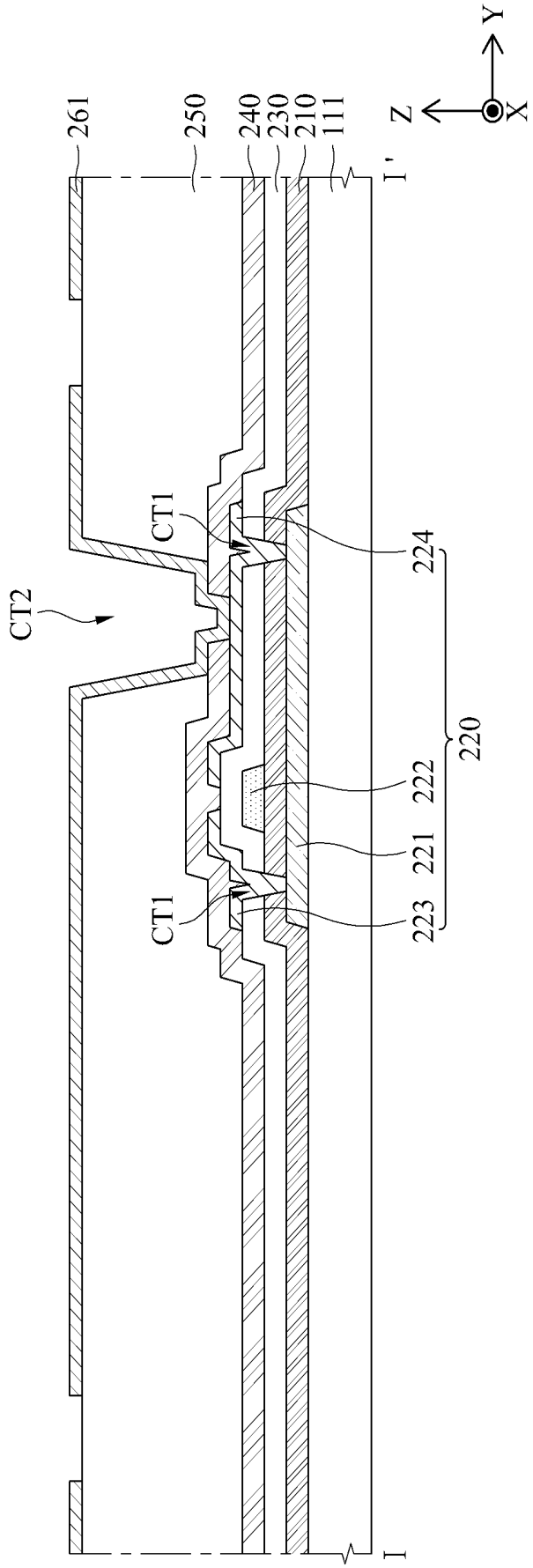

FIG. 9B

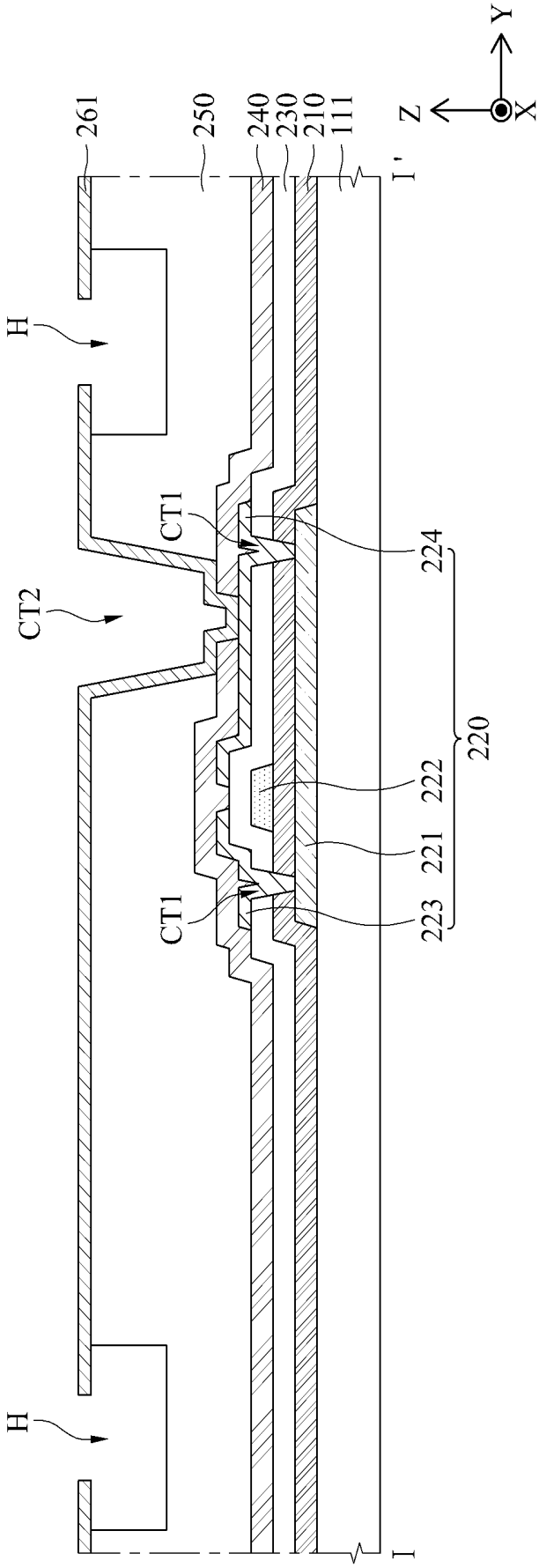

FIG. 9C

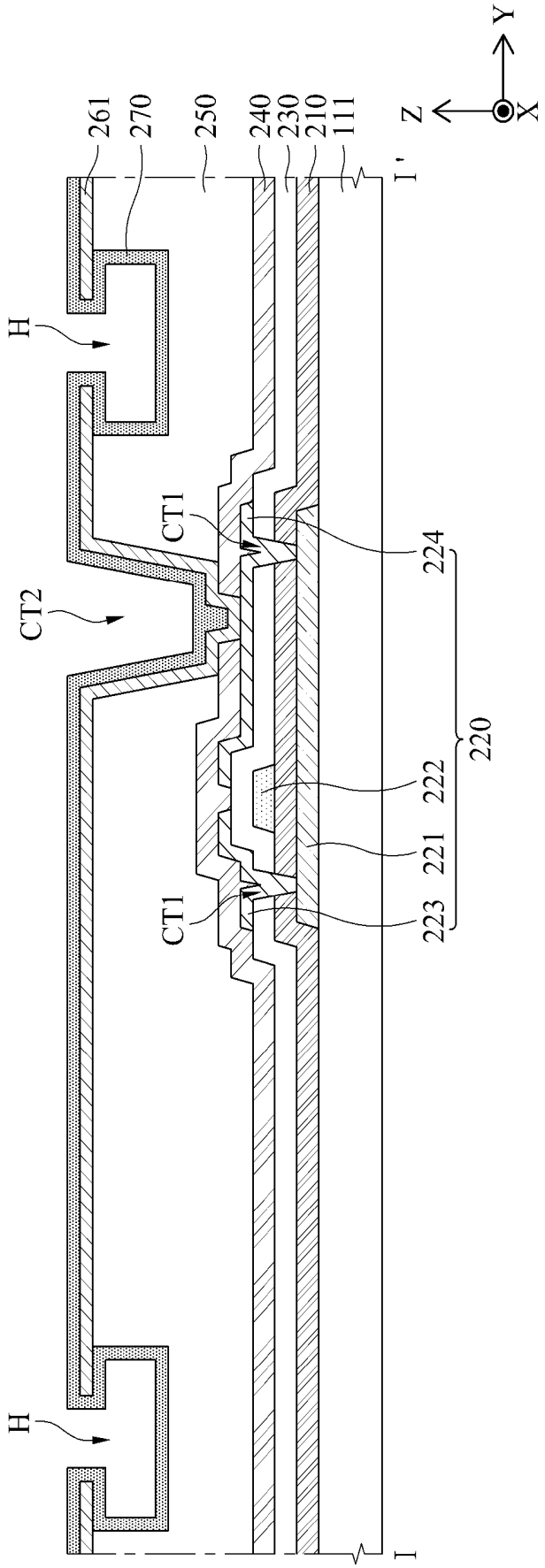
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FIG. 9D

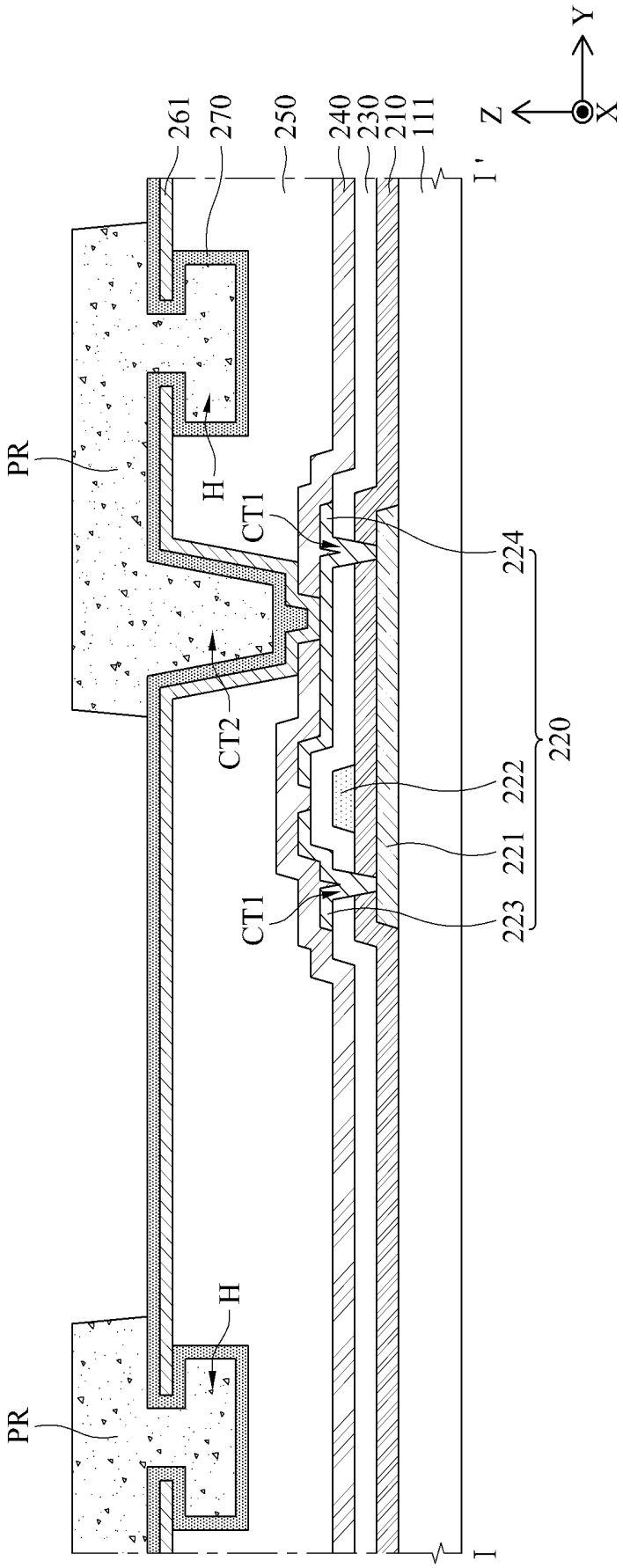
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FIG. 9F

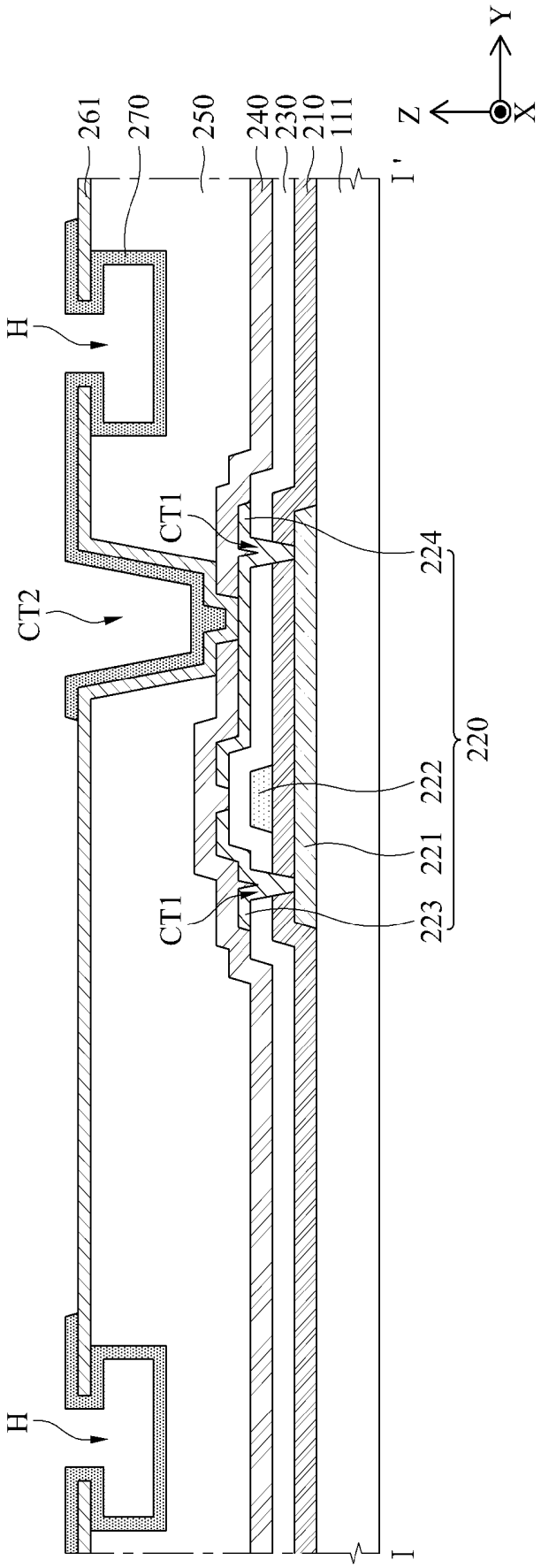
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FIG. 9E

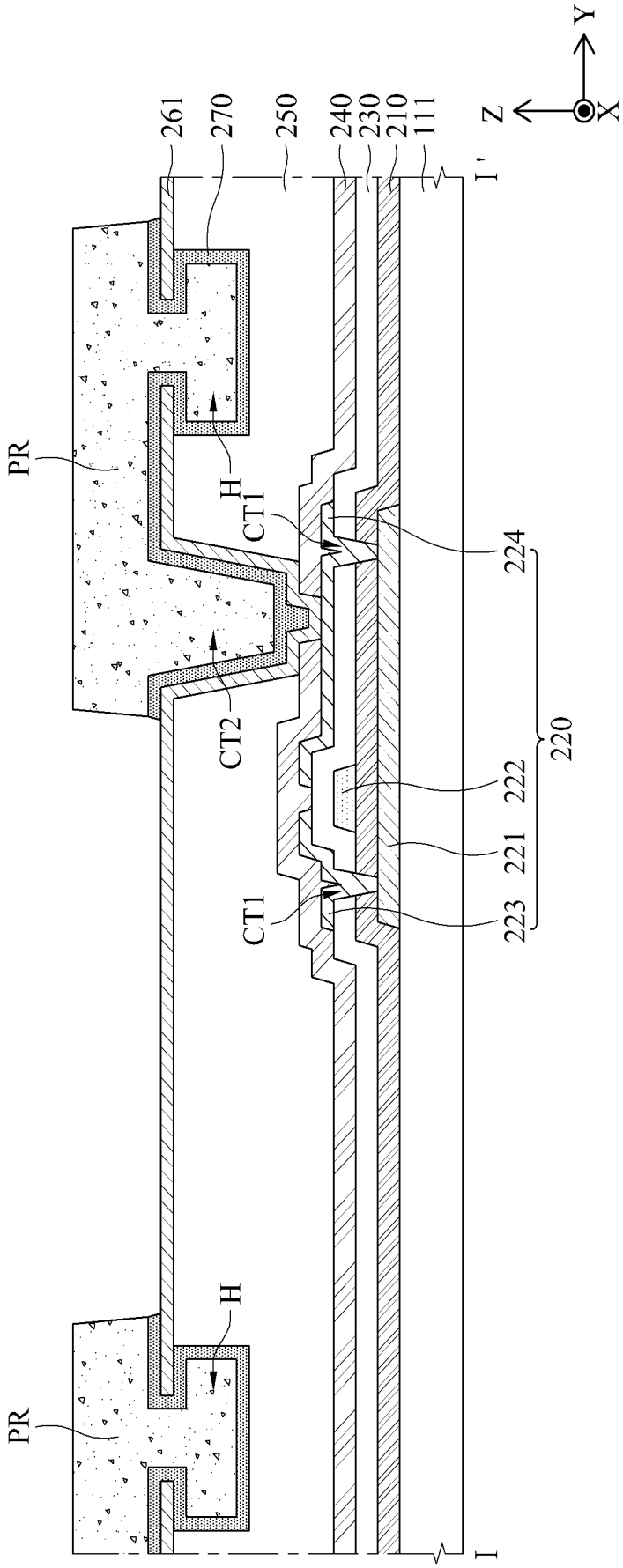
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FIG. 9G

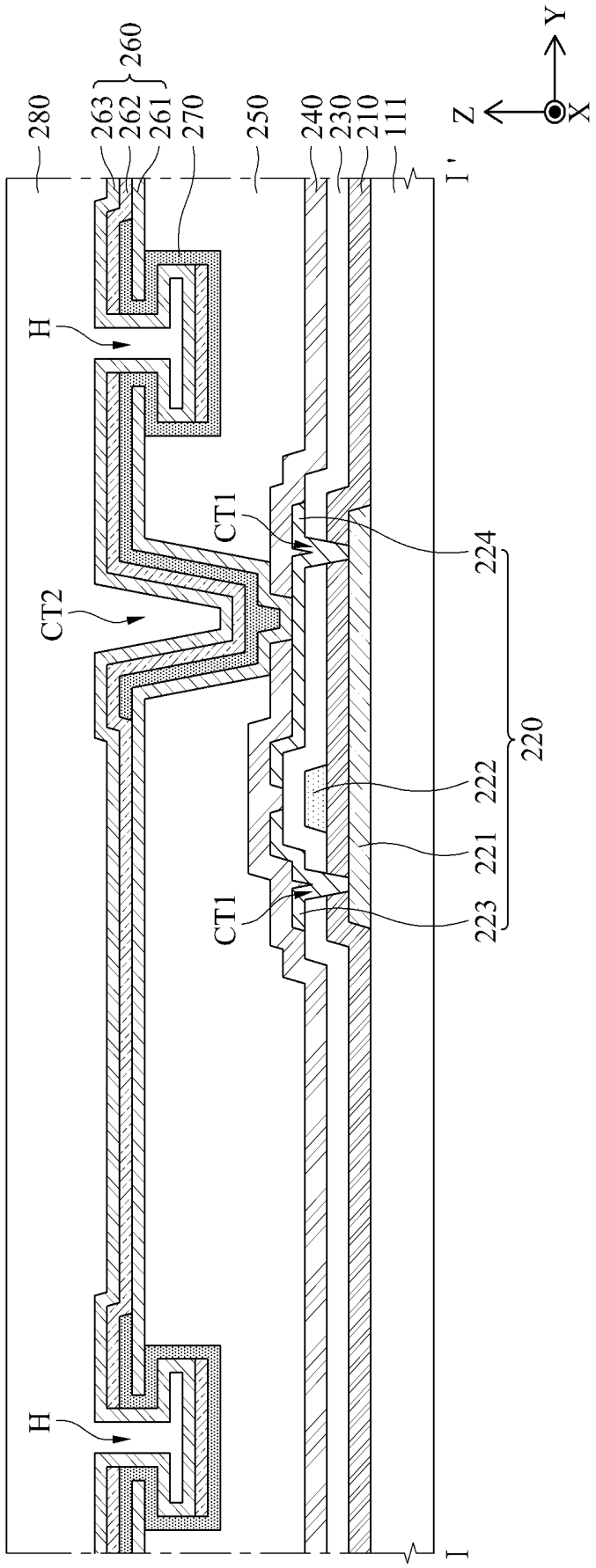
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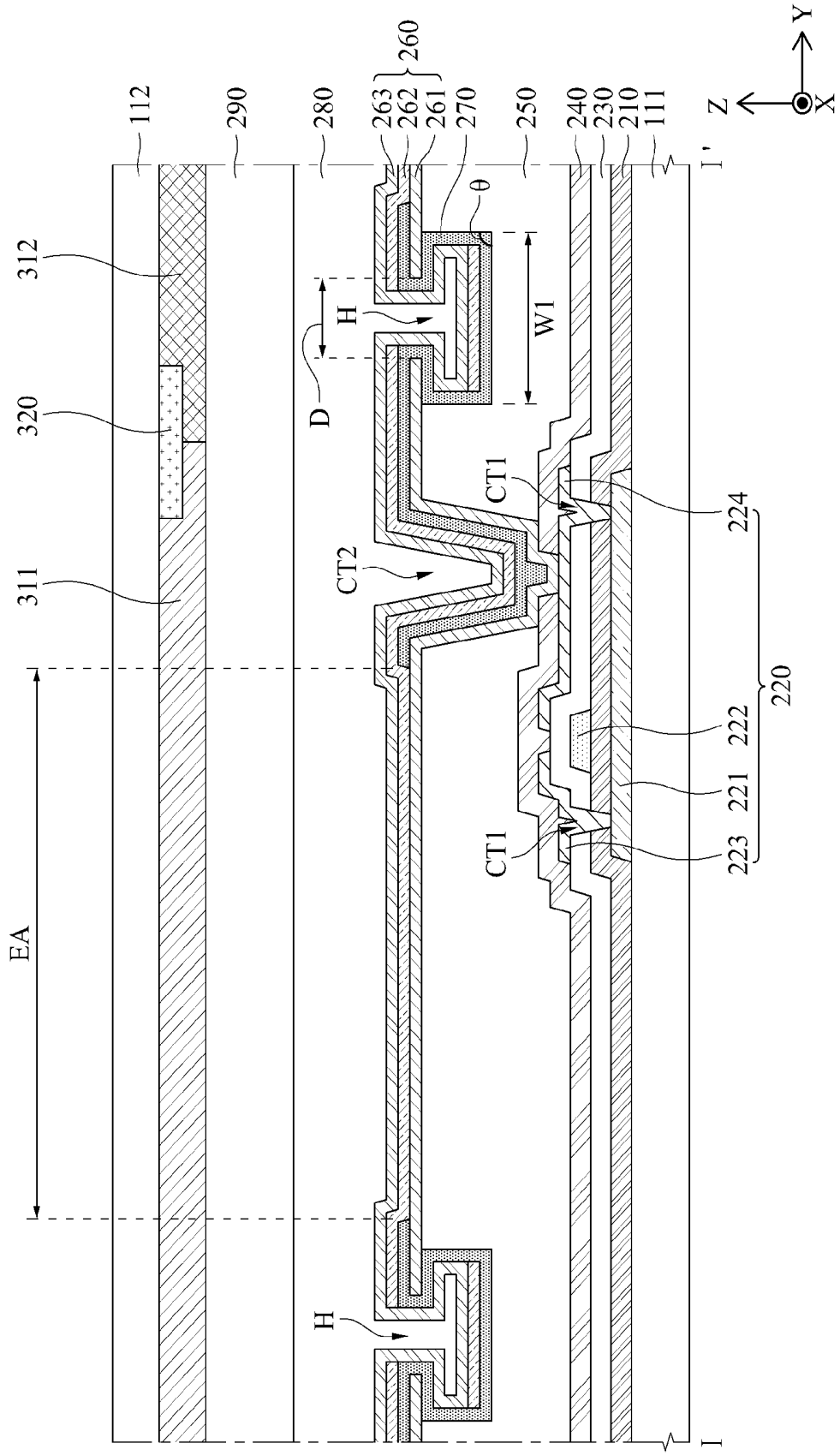
FIG. 9H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ORGANIC LIGHT EMITTING DISPLAY DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the priority benefit of the Korean Patent Application No. 10-2016-0112194 filed on Aug. 31, 2016, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present disclosure relates to an organic light emitting display device and a method of manufacturing the same.

2. Discussion of the Related Art

[0003] With the advancement of information-oriented society, various requirements for display devices for displaying an image are increasing. Therefore, various display devices such as liquid crystal display (LCD) devices, plasma display panel (PDP) devices, organic light emitting display devices, etc. are being used recently.

[0004] As a type of display device, organic light emitting display devices are self-emitting display devices and are better in viewing angle and contrast ratio than LCD devices. Also, since the organic light emitting display devices do not need a separate backlight, it is possible to lighten and make thin the organic light emitting display devices, and the organic light emitting display devices are excellent in power consumption. Furthermore, the organic light emitting display devices are driven with a low direct current (DC) voltage, have a fast response time, and are low in manufacturing cost.

[0005] The organic light emitting display devices each include a plurality of pixels each including an organic light emitting device and a bank which divides the pixels for defining the pixels. The bank may act as a pixel defining layer. The organic light emitting device includes an anode electrode, a hole transporting layer, an organic light emitting layer, and an electron transporting layer, and a cathode electrode. In this instance, when a high-level voltage is applied to the anode electrode and a low-level voltage is applied to the cathode electrode, a hole and an electron respectively move to the organic light emitting layer through the hole transporting layer and the electron transporting layer and are combined with each other in the organic light emitting layer to emit light.

[0006] The organic light emitting device includes a red organic light emitting device emitting red light, a green organic light emitting device emitting green light, and a blue organic light emitting device emitting blue light, or include only a white organic light emitting device emitting white light. If the organic light emitting device includes the white organic light emitting device, the organic light emitting layer and the cathode electrode may be provided in the pixels in common. That is, the organic light emitting layer and the cathode electrode may be connected to each other between adjacent pixels.

[0007] In order to enhance a color reproduction rate and emission efficiency, the white organic light emitting device may be provided in a tandem structure of two or more stacks where two or more organic light emitting layers are stacked. The tandem structure of two or more stacks needs a charge generating layer disposed between adjacent organic light emitting layers. However, in a structure where the organic light emitting layer and the cathode electrode are connected to each other between adjacent pixels, a current can be leaked from one pixel to an adjacent pixel due to the charge generating layer. That is, the adjacent pixel is affected by the leaked current. In this instance, the adjacent pixel cannot emit desired light due to the leaked current, causing a reduction in a color reproduction rate. Particularly, in high-resolution small display devices applied to virtual reality (VR) devices, smartphones, etc., an interval between pixels is narrow, and for this reason, the adjacent pixel is more affected by the leaked current.

SUMMARY OF THE INVENTION

[0008] Accordingly, the present disclosure is directed to provide an organic light emitting display device and a method of manufacturing the same that substantially obviate one or more problems due to limitations and disadvantages of the related art.

[0009] An aspect of the present disclosure is directed to provide an organic light emitting display device and a method of manufacturing the same, in which in a white organic light emitting device, an adjacent pixel is prevented from being affected by a leakage current.

[0010] Additional advantages and features of the disclosure will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the disclosure. The objectives and other advantages of the disclosure may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0011] To achieve these and other advantages and in accordance with the purpose of the disclosure, as embodied and broadly described herein, there is provided an organic light emitting display device including a thin film transistor on a substrate, a planarization layer on the thin film transistor, a contact hole passing through the planarization layer to expose a source or drain electrode of the thin film transistor, a first electrode on the planarization layer, the first electrode being connected to the source or drain electrode of the thin film transistor through the contact hole, a hole between the first electrode and another first electrode adjacent thereto, the hole being a recessed portion of the planarization layer, a pixel defining layer covering the first electrode passing through the contact hole and the planarization layer disposed in the hole, an organic light emitting layer on the first electrode and the pixel defining layer, and a second electrode on the organic light emitting layer.

[0012] In another aspect of the present disclosure, there is provided a method of manufacturing an organic light emitting display device including forming a thin film transistor on a substrate, forming a planarization layer on the thin film transistor, forming a contact hole exposing a source or drain electrode of the thin film transistor through the planarization layer, forming a first electrode connected to the source or drain electrode of the thin film transistor through the contact hole, forming a hole, which is a recessed portion of the planarization layer, between the first electrode and another

first electrode adjacent thereto, forming a pixel defining layer which covers the first electrode passing through the contact hole and the planarization layer disposed in the hole, and sequentially forming an organic light emitting layer, a second electrode, and an encapsulation layer on the first electrode and the pixel defining layer.

[0013] It is to be understood that both the foregoing general description and the following detailed description of the present disclosure are by example and explanatory and are intended to provide further explanation of the disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this application, illustrate embodiments of the disclosure and together with the description serve to explain the principle of the disclosure. In the drawings:

[0015] FIG. **1** is a perspective view illustrating an organic light emitting display device according to an embodiment of the present disclosure;

[0016] FIG. **2** is a plan view illustrating a first substrate, a gate driver, a source drive integrated circuit (IC), a flexible film, a circuit board, and a timing controller of FIG. **1**;

[0017] FIG. **3** is a plan view illustrating an example where a hole and emissive areas of pixels are arranged in a display area according to an embodiment of the present disclosure;

[0018] FIG. **4** is a plan view illustrating another example where a hole and emissive areas of pixels are arranged in a display area according to an embodiment of the present disclosure;

[0019] FIG. **5** is a cross-sectional view illustrating an example taken along line I-I' of FIGS. **3** and **4**;

[0020] FIG. **6** is a cross-sectional view illustrating another example taken along line I-I' of FIGS. **3** and **4**;

[0021] FIG. **7** is a cross-sectional view illustrating another example taken along line I-I' of FIGS. **3** and **4**;

[0022] FIG. **8** is a flowchart illustrating a method of manufacturing an organic light emitting display device according to an embodiment of the present disclosure; and

[0023] FIGS. **9**A to **9**H are cross-sectional views taken along line I-I' of FIGS. **3** and **4** for describing a method of manufacturing an organic light emitting display device according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0024] Reference will now be made in detail to the example embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0025] Advantages and features of the present disclosure, and implementation methods thereof will be clarified through following embodiments described with reference to the accompanying drawings. The present disclosure may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present disclosure to those skilled in the art. Further, the present disclosure is only defined by scopes of claims.

[0026] A shape, a size, a ratio, an angle, and a number disclosed in the drawings for describing embodiments of the present disclosure are merely an example, and thus, the present disclosure is not limited to the illustrated details. Like reference numerals refer to like elements throughout. In the following description, when the detailed description of the relevant known function or configuration is determined to unnecessarily obscure the important point of the present disclosure, the detailed description will be omitted.

[0027] In an instance where 'comprise', 'have', and 'include' described in the present specification are used, another part may be added unless 'only~' is used. The terms of a singular form may include plural forms unless referred to the contrary.

[0028] In construing an element, the element is construed as including an error range although there is no explicit description.

[0029] In describing a position relationship, for example, when a position relation between two parts is described as 'on~', 'over~', 'under~' and 'next~', one or more other parts may be disposed between the two parts unless 'just' or 'direct' is used.

[0030] In describing a time relationship, for example, when the temporal order is described as 'after~', 'subsequent~', 'next~', and 'before~', an instance which is not continuous may be included unless 'just' or 'direct' is used.

[0031] It will be understood that, although the terms "first", "second", etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure.

[0032] An X axis direction, a Y axis direction, and a Z axis direction should not be construed as only a geometric relationship where a relationship therebetween is vertical, and may denote having a broader directionality within a scope where elements of the present disclosure operate functionally.

[0033] The term "at least one" should be understood as including any and all combinations of one or more of the associated listed items. For example, the meaning of "at least one of a first item, a second item, and a third item" denotes the combination of all items proposed from two or more of the first item, the second item, and the third item as well as the first item, the second item, or the third item.

[0034] Features of various embodiments of the present disclosure may be partially or overall coupled to or combined with each other, and may be variously inter-operated with each other and driven technically as those skilled in the art can sufficiently understand. The embodiments of the present disclosure may be carried out independently from each other, or may be carried out together in a co-dependent relationship.

[0035] Hereinafter, example embodiments of the present disclosure will be described in detail with reference to the accompanying drawings.

[0036] FIG. **1** is a perspective view illustrating an organic light emitting display device **100** according to an embodiment of the present disclosure. FIG. **2** is a plan view

illustrating a first substrate, a gate driver, a source drive integrated circuit (IC), a flexible film, a circuit board, and a timing controller of FIG. **1**.

[0037] Referring to FIGS. **1** and **2**, the organic light emitting display device **100** according to an embodiment of the present disclosure may include a display panel **110**, a gate driver **120**, a source drive IC **130**, a flexible film **140**, a circuit board **150**, and a timing controller **160**.

[0038] The display panel **110** may include a first substrate **111** and a second substrate **112**. The second substrate **112** may be an encapsulation substrate. The first substrate **111** and the second substrate **112** may each be plastic, glass, or the like.

[0039] A plurality of gate lines, a plurality of data lines, and a plurality of pixels may be provided on one surface of the first substrate **111** facing the second substrate **112**. The pixels may be respectively provided in a plurality of areas defined by an intersection structure of the gate lines and the date lines.

[0040] Each of the pixels may include a thin film transistor (TFT) and an organic light emitting device which includes a first electrode, an organic light emitting layer, and a second electrode. When a gate signal is input through a gate line, each of the pixels may supply a certain current to the organic light emitting device by using the TFT according to a data voltage supplied through a data line. Therefore, the organic light emitting device of each of the pixels may emit light having certain brightness according to the certain current. A structure of each of the pixels will be described in detail with reference to FIGS. **3** to **6**.

[0041] The display panel **110**, as illustrated in FIG. **2**, may be divided into a display area DA, where the pixels are provided to display an image, and a non-display area NDA which does not display an image. The gate lines, the data lines, and the pixels may be provided in the display area DA. The gate driver **120** and a plurality of pads may be provided in the non-display area NDA.

[0042] The gate driver **120** may sequentially supply gate signals to the gate lines according to a gate control signal input from the timing controller **160**. The gate driver **120** may be provided in the non-display area NDA outside one side or both sides of the display area DA of the display panel **110** in a gate driver-in panel (GIP) type. Alternatively, the gate driver **120** may be manufactured as a driving chip and may be mounted on a flexible film, and moreover, may be attached on the non-display area NDA outside the one side or the both sides of the display area DA of the display panel **110** in a tape automated bonding (TAB) type.

[0043] The source drive IC **130** may receive digital video data and a source control signal from the timing controller **160**. The source driver IC **130** may convert the digital video data into analog data voltages according to the source control signal and may respectively supply the analog data voltages to the data lines. If the source drive IC **130** is manufactured as a driving chip, the source drive IC **130** may be mounted on the flexible film **140** in a chip-on film (COF) type or a chip-on plastic (COP) type.

[0044] A plurality of pads such as data pads may be provided in the non-display area NDA of the display panel **110**. Lines connecting the pads to the source drive IC **130** and lines connecting the pads to lines of the circuit board **150** may be provided on the flexible film **140**. The flexible film **140** may be attached on the pads by using an anisotropic conductive film, and thus, the pads may be connected to the lines of the flexible film **140**.

[0045] The circuit board **150** may be attached on the flexible film **140** which is provided in plurality. A plurality of circuits implemented as driving chips may be mounted on the circuit board **150**. For example, the timing controller **160** may be mounted on the circuit board **150**. The circuit board **150** may be a printed circuit board (PCB) or a flexible printed circuit board (FPCB).

[0046] The timing controller **160** may receive the digital video data and a timing signal from an external system board through a cable of the circuit board **150**. The timing controller **160** may generate a gate control signal for controlling an operation timing of the gate driver **120** and a source control signal for controlling the source drive IC **130** which is provided in plurality, based on the timing signal. The timing controller **160** may supply the gate control signal to the gate driver **120** and may supply the source control signal to the plurality of source drive ICs **130**.

[0047] FIG. **3** is a plan view illustrating an example where a hole and emissive areas of pixels are arranged in a display area. In FIG. **3**, for convenience of description, only a hole H and emissive areas RE, GE, BE, and WE of pixels are illustrated.

[0048] Each of the pixels may include one emissive area. The emissive area may denote an area where a first electrode corresponding to an anode electrode, an organic light emitting layer, and a second electrode corresponding to a cathode electrode are sequentially stacked, and a hole from the first electrode and an electron from the second electrode are combined with each other in the organic light emitting layer to emit light. The first electrode is connected to a thin film transistor through a contact hole CH**1**. The contact hole CH**1** is between each emissive area and the hole H.

[0049] The emissive area may be divided into a red emissive area RE which emits red light by using a red color filter, a green emissive area GE which emits green light by using a green color filter, a blue emissive area BE which emits blue light by using a blue color filter, and a white emissive area WE which emits white light without a color filter. A pixel including the red emissive area RE, a pixel including the green emissive area GE, a pixel including the blue emissive area BE, and a pixel including the white emissive area WE may be defined as one unit pixel.

[0050] The hole H may be disposed to surround each of the emissive areas RE, GE, BE, and WE as in FIG. **3**. Alternatively, as in FIG. **4**, the hole H may be disposed between two adjacent emissive areas of the emissive areas RE, GE, BE, and WE. For this reason, an organic light emitting layer of one pixel may not be connected to an organic light emitting layer of another pixel adjacent to the one pixel. Accordingly, according to an embodiment of the present disclosure, a current is prevented from being leaked from one pixel to another pixel adjacent thereto due to a hole transporting layer and/or a charge generating layer of an organic light emitting layer. That is, according to an embodiment of the present disclosure, the other pixel adjacent to the one pixel is prevented from being affected by the current leaked from the one pixel.

[0051] FIG. **5** is a cross-sectional view illustrating an example taken along line I-I' of FIGS. **3** and **4**.

[0052] Referring to FIG. **5**, a buffer layer may be formed on one surface of the first substrate **111** facing the second

substrate **112**. The buffer layer may be formed on the one surface of the first substrate **111**, for protecting a plurality of TFTs **220** and a plurality of organic light emitting devices **260** from water which penetrates through the first substrate **111** vulnerable to penetration of water. The buffer layer may include a plurality of inorganic layers which are alternately stacked. For example, the buffer layer may be formed of a multilayer where one or more inorganic layers of silicon oxide (SiOx), silicon nitride (SiNx), and SiON are alternately stacked. The buffer layer may be omitted.

[0053] The TFTs **220** may be formed on the buffer layer. Each of the TFTs **220** may include an active layer **221**, a gate electrode **222**, a source electrode **223**, and a drain electrode **224**. In FIG. **5**, the TFTs **220** are by example illustrated as being formed in a top gate type where the gate electrode **222** is disposed on the active layer **221**, but is not limited thereto. In other embodiments, the TFTs **220** may be formed in a bottom gate type where the gate electrode **222** is disposed under the active layer **221** or a double gate type where the gate electrode **222** is disposed both on and under the active layer **221**.

[0054] The active layer **221** may be formed on the buffer layer. The active layer **221** may be formed of a silicon-based semiconductor material or an oxide-based semiconductor material. A light blocking layer for blocking external light incident on the active layer **221** may be formed between the buffer layer and the active layer **221**.

[0055] A gate insulation layer **210** may be formed on the active layer **221**. The gate insulation layer **210** may be formed of an inorganic layer, for example, silicon oxide (SiOx), silicon nitride (SiNx), or a multilayer thereof.

[0056] The gate electrode **222** and a gate line may be formed on the gate insulation layer **210**. The gate electrode **222** and the gate line may each be formed of a single layer or a multilayer which includes one of molybdenum (Mo), chromium (Cr), titanium (Ti), nickel (Ni), neodymium (Nd), and copper (Cu), or an alloy thereof.

[0057] An interlayer dielectric **230** may be formed on the gate electrode **222** and the gate line. The interlayer dielectric **230** may be formed of an inorganic layer, for example, SiOx, SiNx, or a multilayer thereof.

[0058] The source electrode **223**, the drain electrode **224**, and a data line may be formed on the interlayer dielectric **230**. Each of the source electrode **223** and the drain electrode **224** may contact the active layer **221** through a corresponding contact hole CT**1** which passes through the gate insulation layer **210** and the interlayer dielectric **230**. The source electrode **223**, the drain electrode **224**, and the data line may each be formed of a single layer or a multilayer which includes one of Mo, Cr, Ti, Ni, Nd, and Cu, or an alloy thereof.

[0059] A passivation layer **240** for insulating the TFTs **220** may be formed on the source electrode **223**, the drain electrode **224**, and the data line. The passivation layer **240** may be formed of an inorganic layer, for example, SiOx, SiNx, or a multilayer thereof.

[0060] A planarization layer **250** for planarizing a step height caused by the TFTs **220** may be formed on the passivation layer **240**. The planarization layer **250** may be formed of an organic layer such as acryl resin, epoxy resin, phenolic resin, polyamide resin, polyimide resin, and/or the like.

[0061] An organic light emitting device **260** and a pixel defining layer **270** may be formed on the planarization layer **250**. The organic light emitting device **260** may include a first electrode **261**, an organic light emitting layer **262**, and a second electrode **263**. The first electrode **261** may be an anode electrode, and the second electrode **263** may be a cathode electrode.

[0062] The first electrode **261** may be formed on the planarization layer **250**. The first electrode **261** may be connected to the source electrode **223** of the TFT **220** through a contact hole CT**2** which passes through the passivation layer **240** and the planarization layer **250**. The first electrode **261** may be formed of a metal material, having a high reflectivity, such as a stacked structure (Ti/Al/Ti) of aluminum (Al) and titanium (Ti), a stacked structure (ITO/Al/ITO) of Al and ITO, an APC alloy, a stacked structure (ITO/APC/ITO) of an APC alloy and ITO, and/or the like. The APC alloy may be an alloy of Ag, palladium (Pd), and Cu.

[0063] The hole H is provided in the planarization layer. That is, the hole H may be a recessed portion of the planarization layer **250**. The hole H may be formed between adjacent first electrodes **261**. As in FIG. **5**, a width W**1** of the hole H may be set wider than a distance D between the adjacent first electrodes **261**. That is, the hole H may be formed in a pot shape where a width of a floor is wider than that of an entrance. Alternatively, as in FIG. **6**, a width W**2** of the hole H may be set equal to or narrower than the distance D between the adjacent first electrodes **261**. The hole H may be formed in a form of a trench. The hole H may be generally defined as an interruption, a disconnection, or a cut.

[0064] A pixel defining layer **270** may be formed on a portion of the first electrode **261** and in the hole H. For example, the pixel defining layer **270** may be formed on the first electrode **261** in the contact hole CT**2**, the first electrode **261** between the contact hole CT**2** and the hole H. An emissive area EA may be defined as an area where the first electrode **261**, the organic light emitting layer **262**, and the second electrode **263** are sequentially stacked to emit light. The first electrode **261**, the organic light emitting layer **262**, and the second electrode **263** may be sequentially stacked in an area where the pixel defining layer **270** is not provided. Accordingly, the pixel defining layer **270** may divide the emissive area EA to define the emissive area EA.

[0065] The pixel defining layer **270** may be formed in an atomic layer deposition (ALD) process or an initiated chemical vapor deposition (iCVD) process. If the pixel defining layer **270** is formed in the ALD process, the pixel defining layer **270** may be formed to have a thickness of about 0.01 μm to 0.1 μm, and if the pixel defining layer **270** is formed in the iCVD process, the pixel defining layer **270** may be formed to have a thickness of about 0.1 μm to 1 μm. That is, the pixel defining layer **270** may be formed to fill a portion, instead of a whole portion, of the hole H and may be formed to divide the emissive area EA.

[0066] Moreover, a layer formed by the ALD process or the iCVD process is good in step coverage characteristic, and thus, even when the width W**1** of the hole H is set wider than the distance D between the adjacent first electrodes **261** as in FIG. **5**, the pixel defining layer **270** may be formed on both a sidewall and a floor of the hole H. Particularly, the pixel defining layer **270** may also be formed under the first electrode **261**. The step coverage denotes that a layer depos-

ited by a deposition process is continuously connected without being disconnected even in a portion where a step height is formed.

[0067] The organic light emitting layer **262** may be formed on the first electrode **261** and the pixel defining layer **270**. The organic light emitting layer **262** may be a white light emitting layer emitting white light. In this instance, the organic light emitting layer **262** may be formed in a tandem structure of two or more stacks. The two or more stacks may each include a hole transporting layer, at least one light emitting layer, and an electron transporting layer. That is, the organic light emitting layer **282** may include the hole transporting layer, the at least one light emitting layer, and the electron transporting layer.

[0068] Moreover, a charge generating layer may be formed between adjacent stacks. The charge generating layer may include an n-type charge generating layer, disposed adjacent to a lower stack, and a p-type charge generating layer which is formed on the n-type charge generating layer and is disposed adjacent to an upper stack. The n-type charge generating layer may inject an electron into the lower stack, and the p-type charge generating layer may inject a hole into the upper stack. The n-type charge generating layer may be formed of an organic layer which is doped with alkali metal, such as lithium (Li), sodium (Na), potassium (K), or cesium (Cs), or alkali earth metal such as magnesium (Mg), strontium (Sr), barium (Ba), or radium (Ra). The p-type charge generating layer may be an organic layer which is formed by doping a dopant on an organic host material having an ability to transport holes.

[0069] The organic light emitting layer **262** may be formed in a deposition process or a solution process, and if the organic light emitting layer **262** is formed in the deposition process, the organic light emitting layer **262** may be formed in an evaporation process. A layer formed in the evaporation process is not good in step coverage characteristic.

[0070] Therefore, if the width W**1** of the hole H is set wider than the distance D between the adjacent first electrodes **261** as in FIG. **5**, the organic light emitting layer **262** may be disconnectedly formed in the hole H. That is, since the organic light emitting layer **262** is formed in the deposition process which is not good in step coverage characteristic, the organic light emitting layer **262** may be formed on only the floor of the hole H without being formed on the sidewall of the hole H.

[0071] Alternatively, if the width W**2** of the hole H is set equal to or narrower than the distance D between the adjacent first electrodes **261** as in FIG. **6**, a thickness of the organic light emitting layer **262** on the sidewall of the hole H may be set thinner than that of the organic light emitting layer **262** on the floor of the hole H. That is, since an angle "θ" of the sidewall of the hole H is large and the organic light emitting layer **262** is formed in the deposition process which is not good in step coverage characteristic, the organic light emitting layer **262** may be formed thinner on the sidewall of the hole H than the floor of the hole H.

[0072] As a result, since the organic light emitting layer **262** is disconnectedly formed in the hole H due to a step height caused by the hole H, an organic light emitting layer of one pixel may not be connected to an organic light emitting layer of another pixel adjacent to the one pixel. Alternatively, since a thickness of the organic light emitting layer **262** on the sidewall of the hole H is set thinner than that of the organic light emitting layer **262** on the floor of the hole H, a resistance of the organic light emitting layer **262** increases between adjacent pixels. Therefore, according to an embodiment of the present disclosure, the amount of current leaked from one pixel to another pixel adjacent thereto due to the hole transporting layer and/or the charge generating layer of the organic light emitting layer **262** is minimized. Accordingly, according to an embodiment of the present disclosure, the other pixel adjacent to the one pixel is prevented from being affected by the current leaked from the one pixel.

[0073] The angle "θ" of the sidewall of the hole H may be set to 90 degrees or more, but an embodiment of the present disclosure is not limited thereto. That is, the angle "θ" of the sidewall of the hole H may be set to a degree to which since the organic light emitting layer **262** is formed thinner on the sidewall than the floor of the hole H, the resistance of the organic light emitting layer **262** increases, and thus, another pixel adjacent to one pixel is prevented from being affected by a leakage current leaked from the one pixel. For example, the angle "θ" of the sidewall of the hole H may be set to 70 degrees in an instance where even when the angle "θ" of the sidewall of the hole H is 70 degrees, the resistance of the organic light emitting layer **262** increases, and thus, another pixel adjacent to one pixel is prevented from being affected by a leakage current leaked from the one pixel.

[0074] The second electrode **263** may be formed on the organic light emitting layer **262**. The second electrode **263** may be formed of a transparent conductive material (or TCO), such as indium tin oxide (ITO) or indium zinc oxide (IZO) capable of transmitting light, or a semi-transmissive conductive material such as Mg, Ag, or an alloy of Mg and Ag. A capping layer may be formed on the second electrode **263**.

[0075] The second electrode **263** may be formed in a physical vapor deposition (PVD) process such as a sputtering process. A layer formed in the PVD process such as the sputtering process is good in step coverage characteristic. Accordingly, the second electrode **263** may be continuously connected without being disconnected despite a step height caused by the hole H.

[0076] An encapsulation layer **280** may be formed on the second electrode **263**. The encapsulation layer **280** may be formed to fill the contact hole CT**2** and the hole H. That is, in order for the organic light emitting layer **262** to be disconnected in the hole H due to the step height caused by the hole H, the pixel defining layer **270** may be thinly formed by the ALD process or the iCVD process. Therefore, the hole H may be filled not by the pixel defining layer **270** but by the encapsulation layer **280**.

[0077] The encapsulation layer **280** prevents oxygen or water from penetrating into the organic light emitting layer **262** and the second electrode **263**. To this end, the encapsulation layer **280** may include at least one inorganic layer and at least one organic layer.

[0078] For example, the encapsulation layer **280** may include a first inorganic layer, an organic layer, and a second inorganic layer. In this instance, the first inorganic layer may be formed on the second electrode **263** to cover the second electrode **263**. The organic layer may be formed on the first inorganic layer to cover the first inorganic layer. The organic layer may be formed to have a sufficient thickness for preventing particles from penetrating into the organic light emitting layer **262** and the second electrode **263** via the first

inorganic layer. The second inorganic layer may be formed on the organic layer to cover the organic layer.

[0079] The first and second inorganic layers may each be formed of silicon nitride, aluminum nitride, zirconium nitride, titanium nitride, hafnium nitride, tantalum nitride, silicon oxide, aluminum oxide, titanium oxide, and/or the like. The organic layer may be formed of acryl resin, epoxy resin, phenolic resin, polyamide resin, polyimide resin, and/or the like.

[0080] A plurality of color filters **311** and **312** and a black matrix **320** may be formed on one surface of the second substrate **112** facing the first substrate **111**. A red color filter **311** may be formed in a red emissive area RE, a green color filter **312** may be formed in a green emissive area GE, and a blue color filter may be formed in a blue emissive area. The emissive area EA illustrated in FIGS. **5** and **6** may be the red emissive area RE.

[0081] The black matrix **320** may be disposed between the color filters **311** and **312**. The black matrix **320** may be provided in a non-emissive area instead of the emissive area EA, and thus, may be disposed to overlap the pixel defining layer **270**.

[0082] The encapsulation layer **280** of the first substrate **111** may be adhered to the color filters **311** and **312** of the second substrate **112** by using an adhesive layer **290**, and thus, the first substrate **111** may be bonded to the second substrate **112**. The adhesive layer **290** may be a transparent adhesive resin.

[0083] As described above, in an embodiment of the present disclosure, the hole H corresponding to the recessed portion of the planarization layer **250** may be formed between adjacent first electrodes **261**, and the pixel defining layer **270** may be thinly formed by the ALD process or the iCVD process. As a result, according to an embodiment of the present disclosure, since the hole H is not filled with the pixel defining layer **270**, the organic light emitting layer **262** may be disconnected in the hole H due to a step height caused by the hole H, or may be thinly formed on the sidewall of the hole H. Therefore, according to an embodiment of the present disclosure, the amount of current leaked from one pixel to another pixel adjacent thereto due to the hole transporting layer and/or the charge generating layer of the organic light emitting layer is minimized. Accordingly, according to an embodiment of the present disclosure, the other pixel adjacent to the one pixel is prevented from being affected by the current leaked from the one pixel.

[0084] FIG. **7** is a cross-sectional view illustrating another example taken along line I-I' of FIGS. **3** and **4**.

[0085] Except for a pixel defining layer **270**, an organic light emitting display device illustrated in FIG. **7** is substantially as described above with reference to FIGS. **5** and **6**. In FIG. **7**, therefore, detailed descriptions of elements other than the pixel defining layer **270** are omitted.

[0086] Referring to FIG. **7**, the pixel defining layer **270** may be only formed on the first electrode **261** in the contact hole CT**2** and the hole H. Therefore, an emissive area EA where a first electrode **261**, an organic light emitting layer **262**, and a second electrode **263** are sequentially stacked may be provided outside both sides of the contact hole CT**2**, and thus, an area of the emissive area EA may increase. Accordingly, the area of the emissive area EA is enlarged in the organic light emitting display device of FIG. **7** than the organic light emitting display device illustrated in FIGS. **5** and **6**, and thus, an emission efficiency of an organic light emitting device is enhanced.

[0087] FIG. **8** is a flowchart illustrating a method of manufacturing an organic light emitting display device according to an embodiment of the present disclosure. FIGS. **9**A to **9**H are cross-sectional views taken along line I-I' of FIGS. **3** and **4** for describing a method of manufacturing an organic light emitting display device according to an embodiment of the present disclosure. The cross-sectional views illustrated in FIGS. **9**A to **9**H relate to the method of manufacturing the organic light emitting display device illustrated in FIG. **5**, and thus, like reference numerals refer to like elements. Hereinafter, a method of manufacturing an organic light emitting display device according to an embodiment of the present disclosure will be described in detail with reference to FIGS. **8** and **9**A to **9**H.

[0088] First, as in FIG. **9**A, a TFT **220** and a planarization layer **250** may be formed, and a first electrode **261** may be formed on the planarization layer **250**.

[0089] Before the TFT **220** is formed, a buffer layer may be formed on a first substrate **111**, for protecting the TFT **220** from water penetrating through a substrate **100**. The buffer layer may include a plurality of inorganic layers which are alternately stacked, for protecting the TFT **220** and an organic light emitting device **260** from water which penetrates through the first substrate **111** vulnerable to penetration of water. For example, the buffer layer may be formed of a multilayer where one or more inorganic layers of silicon oxide (SiOx), silicon nitride (SiNx), and SiON are alternately stacked. The buffer layer may be formed by using a chemical vapor deposition (CVD) process.

[0090] Subsequently, an active layer **221** of the TFT **220** may be formed on the buffer layer. In detail, an active metal layer may be formed all over the buffer layer by using a sputtering process, a metal organic chemical vapor (MOCVD) process, and/or the like. Subsequently, the active layer **221** may be formed by patterning the active metal layer through a mask process using a photoresist pattern. The active layer **211** may be formed of a silicon-based semiconductor material, an oxide-based semiconductor material, and/or the like.

[0091] Subsequently, a gate insulation layer **210** may be formed on the active layer **221**. The gate insulation layer **210** may be formed of an inorganic layer, for example, silicon oxide (SiOx), silicon nitride (SiNx), or a multilayer thereof.

[0092] Subsequently, a gate electrode **222** of the TFT **220** may be formed on the gate insulation layer **210**. In detail, a first metal layer may be formed all over the gate insulation layer **210** by using a sputtering process, an MOCVD process, and/or the like. Subsequently, the gate electrode **222** may be formed by patterning the first metal layer through a mask process using a photoresist pattern. The gate electrode **222** may be formed of a single layer or a multilayer which includes one of molybdenum (Mo), chromium (Cr), titanium (Ti), nickel (Ni), neodymium (Nd), and copper (Cu), or an alloy thereof.

[0093] Subsequently, an interlayer dielectric **230** may be formed on the gate electrode **222**. The interlayer dielectric **230** may be formed of an inorganic layer, for example, SiOx, SiNx, or a multilayer thereof.

[0094] Subsequently, a plurality of contact holes CT**1** which pass through the gate insulation layer **210** and the interlayer dielectric **230** to expose the active layer **211** may be formed.

[0095] Subsequently, a source electrode **223** and a drain electrode **224** of the TFT **220** may be formed on the interlayer dielectric **230**. In detail, a second metal layer may be formed all over the interlayer dielectric **230** by using a sputtering process, an MOCVD process, and/or the like. Subsequently, the source electrode **223** and the drain electrode **224** may be formed by patterning the second metal layer through a mask process using a photoresist pattern. Each of the source electrode **223** and the drain electrode **224** may contact the active layer **221** through a corresponding contact hole CT**1** which passes through the gate insulation layer **210** and the interlayer dielectric **230**. The source electrode **223** and the drain electrode **224** may each be formed of a single layer or a multilayer which includes one of Mo, Cr, Ti, Ni, Nd, and Cu, or an alloy thereof.

[0096] Subsequently, a passivation layer **240** may be formed on the source electrode **223** and the drain electrode **224** of the TFT **220**. The passivation layer **240** may be formed of an inorganic layer, for example, SiOx, SiNx, or a multilayer thereof. The passivation layer **240** may be formed by using a CVD process.

[0097] Subsequently, a planarization layer **250** for planarizing a step height caused by the TFT **220** may be formed on the passivation layer **240**. The passivation layer **250** may be formed of an organic layer such as acryl resin, epoxy resin, phenolic resin, polyamide resin, polyimide resin, and/or the like.

[0098] Subsequently, a first electrode **261** of the organic light emitting device **260** may be formed on the planarization layer **250**. In detail, a third metal layer may be formed all over the planarization layer **250** by using a sputtering process, an MOCVD process, and/or the like. Subsequently, the first electrode **261** may be formed by patterning the third metal layer through a mask process using a photoresist pattern. The first electrode **261** may be connected to the source electrode **223** of the TFT **220** through a contact hole CT**2** which passes through the passivation layer **240** and the planarization layer **250**. The first electrode **261** may be formed of a metal material, having a high reflectivity, such as a stacked structure (Ti/Al/Ti) of aluminum (Al) and titanium (Ti), a stacked structure (ITO/Al/ITO) of Al and ITO, an APC alloy, a stacked structure (ITO/APC/ITO) of an APC alloy and ITO, and/or the like (S**101** of FIG. **8**).

[0099] Second, as in FIG. **9**B, a hole H corresponding to a recessed portion of the planarization layer **250** may be formed between adjacent first electrodes **261**. In detail, by dry-etching the planarization layer **250** with the first electrodes **261** as a mask, the hole H corresponding to the recessed portion of the planarization layer **250** may be formed between the adjacent first electrodes **261**. A material applied to the dry-etching may be O_2 or a mixed gas of O_2 and CF_4.

[0100] As in FIG. **5**, a width W**1** of the hole H may be set wider than a distance D between the adjacent first electrodes **261**. Alternatively, as in FIG. **6**, a width W**2** of the hole H may be set equal to or narrower than the distance D between the adjacent first electrodes **261** (S**102** of FIG. **8**).

[0101] Third, as in FIG. **9**C, a pixel defining layer **270** may be formed on the planarization layer **250** disposed in the hole H and the first electrode **261**. That is, the pixel defining layer **270** may be formed all over the first substrate **111**. The pixel defining layer **270** may be an insulation layer.

[0102] The pixel defining layer **270** may be formed in an atomic layer deposition (ALD) process or an initiated chemical vapor deposition (iCVD) process. If the pixel defining layer **270** is formed in the ALD process, the pixel defining layer **270** may be formed to have a thickness of about 0.01 μm to 0.1 μm, and if the pixel defining layer **270** is formed in the iCVD process, the pixel defining layer **270** may be formed to have a thickness of about 0.1 μm to 1 μm.

[0103] A layer formed in the ALD process or the iCVD process is good in step coverage characteristic. Therefore, a layer formed by the ALD process or the iCVD process is good in step coverage characteristic, and thus, even when the width W**1** of the hole H is set wider than the distance D between the adjacent first electrodes **261** as in FIG. **5**, the pixel defining layer **270** may be formed on both a sidewall and a floor of the hole H. Particularly, the pixel defining layer **270** may also be formed under the first electrode **261**. That is, the pixel defining layer **270** may be continuously connected without being disconnected despite a step height caused by the hole H (S**103** of FIG. **8**).

[0104] Fourth, as in FIG. **9**D, a photoresist pattern PR may be formed on the pixel defining layer **270**. The photoresist pattern PR may be formed in an area other than an emissive area EA (S**104** of FIG. **8**).

[0105] Fifth, as in FIG. **9**E, the pixel defining layer **270** uncovered by the photoresist pattern PR may be dry-etched. Therefore, a portion of the first electrode **261** corresponding to the emissive area EA may be exposed (S**105** of FIG. **8**).

[0106] Sixth, as in FIG. **9**F, the photoresist pattern PR may be removed (S**106** of FIG. **8**).

[0107] Seventh, as in FIG. **9**G, an organic light emitting layer **262**, a second electrode **263**, and an encapsulation layer **280** may be sequentially formed on the first electrode **261** and the pixel defining layer **270**.

[0108] In detail, the organic light emitting layer **262** may be formed on the first electrode **261** and the pixel defining layer **270** in a deposition process or a solution process. If the organic light emitting layer **262** is formed in the deposition process, the organic light emitting layer **262** may be formed in an evaporation process. A layer formed in the evaporation process is not good in step coverage characteristic.

[0109] Therefore, if the width W**1** of the hole H is set wider than the distance D between the adjacent first electrodes **261** as in FIG. **5**, the organic light emitting layer **262** may be disconnectedly formed in the hole H. That is, since the organic light emitting layer **262** is formed in the deposition process which is not good in step coverage characteristic, the organic light emitting layer **262** may be formed on only the floor of the hole H without being formed on the sidewall of the hole H.

[0110] Alternatively, if the width W**2** of the hole H is set equal to or narrower than the distance D between the adjacent first electrodes **261** as in FIG. **6**, a thickness of the organic light emitting layer **262** on the sidewall of the hole H may be set thinner than that of the organic light emitting layer **262** on the floor of the hole H. That is, since an angle "θ" of the sidewall of the hole H is large and the organic light emitting layer **262** is formed in the deposition process which is not good in step coverage characteristic, the organic light emitting layer **262** may be formed thinner on the sidewall of the hole H than the floor of the hole H.

[0111] As a result, since the organic light emitting layer **262** is disconnectedly formed in the hole H due to a step height caused by the hole H, an organic light emitting layer of one pixel may not be connected to an organic light emitting layer of another pixel adjacent to the one pixel. Alternatively, since a thickness of the organic light emitting layer **262** on the sidewall of the hole H is set thinner than that of the organic light emitting layer **262** on the floor of the hole H, a resistance of the organic light emitting layer **262** increases between adjacent pixels. Therefore, according to an embodiment of the present disclosure, the amount of current leaked from one pixel to another pixel adjacent thereto due to the hole transporting layer and/or the charge generating layer of the organic light emitting layer **262** is minimized. Accordingly, according to an embodiment of the present disclosure, the other pixel adjacent to the one pixel is prevented from being affected by the current leaked from the one pixel.

[0112] Subsequently, the second electrode **263** may be formed on the organic light emitting layer **262**. The second electrode **263** may be formed of a transparent conductive material (or TCO), such as indium tin oxide (ITO) or indium zinc oxide (IZO) capable of transmitting light, or a semi-transmissive conductive material such as Mg, Ag, or an alloy of Mg and Ag. The second electrode **263** may be formed in a physical vapor deposition (PVD) process such as a sputtering process. A layer formed in the PVD process such as the sputtering process is good in step coverage characteristic. Accordingly, the second electrode **263** may be continuously connected without being disconnected despite a step height caused by the hole H.

[0113] Subsequently, a capping layer may be formed on the second electrode **263**.

[0114] Subsequently, an encapsulation layer **280** may be formed on the second electrode **263**. The encapsulation layer **280** may be formed to fill the contact hole CT**2** and the hole H.

[0115] The encapsulation layer **280** prevents oxygen or water from penetrating into the organic light emitting layer **262** and the second electrode **263**. To this end, the encapsulation layer **280** may include at least one inorganic layer and at least one organic layer.

[0116] For example, the encapsulation layer **280** may include a first inorganic layer, an organic layer, and a second inorganic layer. In this instance, the first inorganic layer may be formed on the second electrode **263** to cover the second electrode **263**. The organic layer may be formed on the first inorganic layer to cover the first inorganic layer. The organic layer may be formed to have a sufficient thickness for preventing particles from penetrating into the organic light emitting layer **262** and the second electrode **263** via the first inorganic layer. The second inorganic layer may be formed on the organic layer to cover the organic layer.

[0117] The first and second inorganic layers may each be formed of silicon nitride, aluminum nitride, zirconium nitride, titanium nitride, hafnium nitride, tantalum nitride, silicon oxide, aluminum oxide, titanium oxide, and/or the like. The organic layer may be formed of acryl resin, epoxy resin, phenolic resin, polyamide resin, polyimide resin, and/or the like (S**107** of FIG. **8**).

[0118] Eighth, as in FIG. **9**H, the encapsulation layer **280** of the first substrate **111** may be adhered to the color filters **311** and **312** of the second substrate **112** by using an adhesive layer **290**. Therefore, the first substrate **111** may be bonded to the second substrate **112**. The adhesive layer **290** may be a transparent adhesive resin (S**108** of FIG. **8**).

[0119] As described above, in an embodiment of the present disclosure, the hole H corresponding to the recessed portion of the planarization layer **250** may be formed between adjacent first electrodes **261**, and the pixel defining layer **270** may be thinly formed by the ALD process or the iCVD process. As a result, according to an embodiment of the present disclosure, since the hole H is not filled with the pixel defining layer **270**, the organic light emitting layer **262** may be disconnected in the hole H due to a step height caused by the hole H, or may be thinly formed on the sidewall of the hole H. Therefore, according to an embodiment of the present disclosure, the amount of current leaked from one pixel to another pixel adjacent thereto due to the hole transporting layer and/or the charge generating layer of the organic light emitting layer is minimized. Accordingly, according to an embodiment of the present disclosure, the other pixel adjacent to the one pixel is prevented from being affected by the current leaked from the one pixel.

[0120] Moreover, according to the embodiments of the present disclosure, the hole may be formed in order for the planarization layer to be recessed between the first electrodes, and the pixel defining layer may be thinly formed by the ALD process or the iCVD process. As a result, according to the embodiments of the present disclosure, since the hole is not filled with the pixel defining layer, the organic light emitting layer may be disconnected in the hole due to a step height caused by the hole, or may be thinly formed on a sidewall of the hole. Therefore, according to the embodiments of the present disclosure, the amount of current leaked from one pixel to another pixel adjacent thereto due to the hole transporting layer and/or the charge generating layer of the organic light emitting layer is minimized. Accordingly, according to the embodiments of the present disclosure, the other pixel adjacent to the one pixel is prevented from being affected by the current leaked from the one pixel.

[0121] It will be apparent to those skilled in the art that various modifications and variations can be made in the present disclosure without departing from the spirit or scope of the disclosures. Thus, it is intended that the present disclosure covers the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An organic light emitting display device comprising:

a plurality of emissive areas each having a first electrode, a light emitting layer on the first electrode, and a second electrode on the light emitting layer; and

a hole between a first emissive area and a second emissive area of the plurality of emissive areas to disconnect the light emitting layer of the first emissive area from the light emitting layer of the second emissive area.

2. The organic light emitting display device of claim **1**, further comprising:

a substrate;

a thin film transistor on the substrate;

a planarization layer on the thin film transistor; and

a contact hole passing through the planarization layer to expose a source or drain electrode of the thin film transistor.

3. The organic light emitting display device of claim **2**, wherein one first electrode is on the planarization layer, and is connected to the source or drain electrode of the thin film

transistor through the contact hole, and wherein the hole is provided in the planarization layer.

4. The organic light emitting display device of claim **3**, further comprising a pixel defining layer both on a portion of the one first electrode and in the hole.

5. The organic light emitting display device of claim **4**, wherein the pixel defining layer is provided on both a side wall and a floor of the hole.

6. The organic light emitting display device of claim **5**, wherein a portion of the light emitting layer is provided on the floor of the hole.

7. The organic light emitting display device of claim **1**, wherein the hole is between one first electrode of the first emissive area and one second electrode of the second emissive area.

8. The organic light emitting display device of claim **1**, wherein a width of the hole is wider than a distance between one first electrode of the first emissive area and one first electrode of the second emissive area.

9. The organic light emitting display device of claim **4**, wherein one second electrode is provided on the pixel defining layer in the hole.

10. The organic light emitting display device of claim **1**, wherein a width of the hole is equal to or narrower than a distance between one first electrode of the first emissive area and one first electrode of the second emissive area.

11. The organic light emitting display device of claim **6**, wherein a thickness of the portion of the light emitting layer on a sidewall of the hole is thinner than a thickness of the portion of the light emitting layer on the floor of the hole.

12. The organic light emitting display device of claim **4**, wherein the pixel defining layer fills a portion of the hole.

13. The organic light emitting display device of claim **4**, further comprising an encapsulation layer on one second electrode, the encapsulation layer filling the contact hole and the hole.

14. The organic light emitting display device of claim **13**, further comprising:

a plurality of color filters on the encapsulation layer; and

a black matrix between adjacent color filters, the black matrix overlapping the pixel defining layer.

15. The organic light emitting display device of claim **14**, wherein the hole is aligned with the black matrix.

16. The organic light emitting display device of claim **4**, wherein the plurality of emissive areas are divided by the pixel defining layer.

17. The organic light emitting display device of claim **1**, wherein the hole is disposed to surround an emissive area of the plurality of emissive areas.

18. The organic light emitting display device of claim **2**, wherein the contact hole is between an emissive area of the plurality of emissive areas and the hole.

19. A method of manufacturing an organic light emitting display device, the method comprising:

forming a thin film transistor on a substrate, the substrate having a plurality of emissive areas;

forming a planarization layer on the thin film transistor;

forming a contact hole exposing a source or drain electrode of the thin film transistor through the planarization layer;

forming a first electrode connected to the source or drain electrode of the thin film transistor through the contact hole;

forming a hole between adjacent emissive areas, the hole being provided in the planarization layer;

forming a pixel defining layer on a portion of the first electrode and in the hole; and

sequentially forming a light emitting layer, a second electrode, and an encapsulation layer on the first electrode and the pixel defining layer.

20. The method of claim **19**, wherein the forming of the pixel defining layer comprises:

forming the pixel defining layer on the portion of the first electrode and in the hole by using an atomic layer deposition (ALD) process or an initiated chemical vapor deposition (iCVD) process;

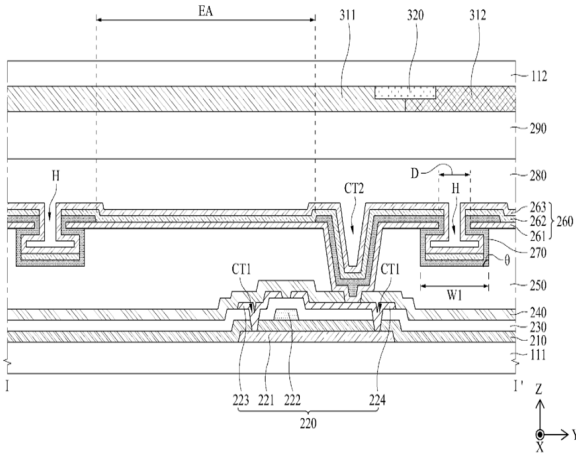
forming a photoresist pattern on the pixel defining layer;

etching the pixel defining layer uncovered by the photoresist pattern to expose the portion of the first electrode; and

removing the photoresist pattern.

* * * * *

专利名称(译)	有机发光显示装置及其制造方法		
公开(公告)号	US20180061907A1	公开(公告)日	2018-03-01
申请号	US15/669489	申请日	2017-08-04
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KIM JONGSUNG HEO JOONYOUNG		
发明人	KIM, JONGSUNG HEO, JOONYOUNG		
IPC分类号	H01L27/32 H01L51/52		
CPC分类号	H01L27/3213 H01L27/322 H01L51/5237 H01L51/5284 H01L27/3246 H01L27/3211 H01L27/3244 H01L51/56 H01L27/3258 H01L51/5012		
优先权	1020160112194 2016-08-31 KR		
其他公开文献	US10553652		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种有机发光显示装置，包括在基板上的薄膜晶体管，在薄膜晶体管上的平坦化层，穿过平坦化层以暴露薄膜晶体管的源极或漏极的接触孔，第一电极在平坦化层上，第一电极通过接触孔连接到薄膜晶体管的源极或漏极，第一电极和与其相邻的另一个第一电极之间的孔，该孔是平坦化层的凹陷部分，像素限定层覆盖穿过接触孔的第一电极和设置在孔中的平坦化层，第一电极和像素限定层上的发光层，以及发光层上的第二电极。